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GitHub - ultraembedded/core_ddr3_controller:

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compatible with the DDR4 and DDR3 standards. The PHY consists of a Command/Address (C/A) macro cell and Data (DQ) macro cells configured to create a 72-bit wide channel.

DDR4 Controller / Interface IP - Rambus

Figure 1-1 on page 1-1 shows a system-level diagram including the example top-level file that the DDR3 SDRAM Controller with ALTMEMPHY IP creates for you. The MegaWizard™ Plug-In Manager generates an example top-level file, consisting of an example driver, and your DDR3 SDRAM high-performance controller custom variation.

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