

## Dc Shell User Guide

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Acces PDF Dc Shell User Guide Dc Shell User Guide v1999.10 Design Compiler User Guide dc\_shell> write -hierarchy -output my\_design.db To exit dc\_shell, do one of the following: • Enter quit. • Enter exit. • Press Ctrl-d. When you exit dc\_shell, text similar to the following appears (the memory and the CPU numbers reflect your actual usage): Memory

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The following command tells # the tool that the pin named clk is the clock and that the desired clock # period is 1 nanosecond. dc\_shell-topo> create\_clock clk -name ideal\_clock1 -period 1 # The compile\_ultra command begins the actuall synthesis process that # transforms your design into a gate-level netlist.

**RTL-to-Gates Synthesis using Synopsys Design Compiler**

4 User Commands dc\_shell-t Invokes the Design Compiler shell in dctcl mode. For more information, see the man page for dc\_shell. dc\_shell-t [-f script\_file] [-x command\_string] [-no\_init] [-checkout feature\_list] [-wait wait\_time] [-timeout timeout\_value] [-version] [-behavioral] [-fpga] [-syntax\_check | -context\_check] dc\_shell

**Synthesis Quick Reference - Computer Science**

dc\_shell -f scriptFile Most efficient and common usage is to put TCL commands into scriptFile ,including "quit" at the end TCL = Tool Command Language Edit and rerun scriptFile as needed GUI version (Design Vision) design\_vision From dc\_shell: gui\_start Main advantage over dc\_shell is to view the synthesized schematic

**Automated Synthesis from HDL models**

CS250 Tutorial 5 (Version 091210b) September 12, 2010 Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

**RTL-to-Gates Synthesis using Synopsys Design Compiler**

For more information on the compile command consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileat the DC shell prompt. Run the following command and take a look at the output. dc\_shell-xg-t> compile -map\_effort medium -area\_effort medium The compile command will report how the design is being optimized.

**RTL-to-Gates Synthesis using Synopsys Design Compiler**

the compileultracommmand consult the Design Compiler User Guide (dc-user-guide.pdf) or use man compileultraat the DC shell prompt. Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints. DC considers two

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Questions [Book] Dc Shell User Guide Acces PDF Dc Shell User Guide dc\_shell. The dc\_shell supports two scripting languages - dcsh, which uses the Synopsys language, and dctcl, which uses Tcl (Tool Command Language). It is recommended that Design Analyzer be used for most of the synthesis and optimization processes. The dc\_shell is preferable for a standardized synthesis Dc Shell User Guide - glascentrale-nederland.nl Dc Shell User Guide Dc Shell User Guide If

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%> dc shell -t any memory LIB file %> dc\_shell dc\_shell-t> read\_lib t13spsram512x32\_slow\_syn.lib dc\_shell-t> write\_lib t13spsram512x32 -output \ t13spsram512x32\_slow\_syn.db Modify <.synopsys\_dc.setup> File: "\*" user library name, which should be the same as the library name in the Artisan set link\_library slow.db t13spsram512x32\_slow.db

**Training Course of Design Compiler [????]**

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View Dc\_shell commands from ELECTRONICS 121 at Rajasthan Technical University. # #Design Compiler settings can be in .synopsys\_dc.setup # #Reading design file read\_verilog golden\_arbiter.v #Pointing

**Dc\_shell commands - #Design Compiler settings can be in ...**

Figure 1.1 Workflow of DC We use Synopsys Design Compiler (DC) to synthesize Verilog RTL models into a gate-level netlist where all of the gates are from the standard cell library. So Synopsys DC ... % dc\_shell-t -f <file>.tcl In the above example, it should be: % dc\_shell-t -f compiledc.tcl

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In the preceding example, a dedicated wrapper cell is used. Chapter 8: Wrapping Cores Core Wrapping Flows 8-13 DFT Compiler Scan User Guide Version H-2013.03-SP4 To prevent the insertion of wrapper cells for a specific list of ports, use the following command: dc\_shell> set\_boundary\_cell -class core\_wrapper \ -ports port\_list -type none This might be needed in cases where an output port drives downstream clock pins or asynchronous set or reset signals.

**dcshell set linklibrary mytechlibdb dwfoundationsldb ...**

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